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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,762	11/19/2001	Kenneth Y. Ogami	CYPR-CD01175M	2087
7590 07/23/2007 WAGNER, MURABITO & HAO LLP Third Floor Two North Market Street San Jose, CA 95113			EXAMINER OSBORNE, LUKE R	
			ART UNIT 2123	PAPER NUMBER
			MAIL DATE 07/23/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

09/989,762

Applicant(s)

OGAMI ET AL.

Examiner

Luke Osborne

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2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/26/2007 has been entered.

***Claim Status***

2. Claims 1-37 have been presented for reconsideration.

Claims 1-37 are now pending in the instant application.

Applicants' arguments submitted 4/26/2007 have been fully considered, Examiners response is as follows.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 10-37 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,757,882 to Chen et al. hereinafter "Chen".

Regarding claim 1, Chen discloses a method of matching selectable user module with a plurality of programmable hardware resources associated with a programmable integrated circuit (See the tool as shown in figure 4).

displaying said selectable user module [Chen: Figure 7, items 710 a designer 202 first selects the memory components to be employed from a provided list of available memory items. (Column 14, lines 20-30)], wherein said user module is representation of a configuration of a programmable circuit for implementation on said programmable integrated circuit;

in response to a selection of said selectable user module, comparing a description of a hardware resource requirement of said selectable user module with a description of said plurality of programmable hardware resources associated with said programmable integrated circuit [Chen: Column 12, line 31-Column 13, line 26]; and

in response to said comparing to identify and to display a first allowed programmable hardware resource of the programmable integrated circuit satisfying the hardware resource requirement of said programmable circuit of said selectable user module wherein said first allowed programmable hardware

resource is graphically corresponded to said selectable user module [Chen: Figures 7-11, (Column 14, lines 20-30) the compatible devices for placement are in the top right of the figures].

### **Applicant's Argue**

Chen fails to teach or suggest "in response to a selection of the selectable user module, comparing a description of a hardware resource requirement of the selectable user module with a description of the plurality of programmable hardware resources as claimed.

Chen fails to teach or suggest "graphically corresponding" as claimed.

### **Examiners Response**

The Examiner has considered Applicant's response unpersuasive. Rather as disclosed by Chen

The present invention also contemplates support for SOC designs that employ a secondary bus that is not part of the nucleus of the design. Designers 202 are also able to use the features of Tool Suite 204 to add components to the SOC design that are general-purpose peripherals. General-purpose peripherals are those that do not reside on a high-speed bus. For example, in one SOC design, where a designer 202 has chosen an Ericsson Bluetooth ARM7TDMI processor supporting AMBA 2.0, the AMBA Advanced Peripheral Bus may also be chosen as the general-purpose bus for attaching other I/O peripheral devices. In a manner similar to that discussed above with respect to the AHB, a user may explicitly or implicitly choose a general-purpose bus type. With this information, a list of available peripherals components that support the Advanced Peripheral Bus is ascertained. A designer 202 may then be provided with the determined list of these available components for selection. Column 12 line 54 – Column 13, line 4. This also allows for the user to select an IP block that was not given in the list from the list presented to the user.

In regard to the alleged lack of support for "graphically corresponding" the Examiner does not recognize "graphically corresponding" as a term of art and Applicant's have not provided a specific definition for the term. As such the broadest

reasonable interpretation is that the selection is reflected in the work area of the designers GUI. This is disclosed in Chen Column 13 lines 5-26. Furthermore this feature is disclosed in the previously cited PSOC designer on page 33.

Regarding claim 2 Chen discloses wherein the description of the hardware resource requirement of the user module is represented as XML [Chen: For the embodiment, description 210' is expressed using a XML-like Language having XML like language tags defined in accordance with a schema of a namespace associated with Tool Suite 204 (Column 8, lines 23-35)].

Regarding claim 3, Chen discloses wherein the description of the plurality of said selectable programmable resources are represented as XML data [Chen: For the embodiment, description 210' is expressed using a XML-like Language having XML like language tags defined in accordance with a schema of a namespace associated with Tool Suite 204 (Column 8, lines 23-35)].

Regarding claim 4, Chen discloses the method according to Claim 1 further comprising highlighting the first allowed programmable hardware resource using a graphical user interface [Chen: Upon determining the information, in like manner, bus compatibility analyzer 254 stores the supported bus architecture information, including related synthesized information, into database 260, block 1312 along with figure 6].

### **Applicant's Argue**

Chen fails to teach or suggest highlighting, as claimed.

### **Examiners Response**

The Examiner has considered Applicant's arguments and found them unpersuasive. Chen discloses

For a given base platform design, when it is selected for the SOC design, a customization/configuration menu/form appears, which prompts the designer 202 for inputs for the customizable or configurable attributes of the base platform. Recall that as part of the acquisition process, customizable attribute or parameter information and if applicable, UI element descriptions are read and stored in database 260. In response to the selection of a base platform, the customizable attribute or parameter information, including application UI element descriptions, are retrieved, and customization input forms for prompting a designer 202 to supply the attribute or parameter values are dynamically generated and presented to the designer 202 in order. Column 13, lines 27-39 and as seen from Figure 6 the first option is highlighted.

Furthermore, previously referenced PSOC Designer on page 33 also discloses this feature.

Regarding claim 5, Chen discloses identifying a second allowed programmable hardware resource for use with the invention. [Chen: Figure 7 shows a plurality of memory devices that satisfy the hardware resource of the core being used].

Claim 6 discloses a similar limitation to Claim 4 thus is rejected for the same reasons as claim 4.

Regarding claim 7, Chen discloses the method according to Claim 1 further comprising identifying a disallowed programmable resource associated with said programmable integrated circuit wherein the disallowed resource represents and

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unavailable resource associated with said programmable integrated circuit that otherwise satisfies the hardware resource requirement of said selectable user module [In response, bus compatibility analyzer 254 determines the bus architectures supported accordingly, including bus signals implemented, and disposition/handling of the unimplemented signals, block 1310 (Column 10, lines 4-16) when determining what is allowable the disallowed resources are identified].

Regarding claim 10, Chen discloses the method according to Claim 1 further comprising updating the description of the hardware resource requirement of said selectable user module

[Chen: Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31]

Regarding claim 11, Chen discloses the method according to Claim 10 wherein said updating is performed in response to changes in a hardware resource requirement of said selectable user module.

[Chen: Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31]



Regarding claim 12, Chen discloses the method according to Claim 1 further comprising adding an additional selectable user module to the description of the hardware resource requirement of said selectable user module.

[Chen: In alternate embodiments, Tool Suite 204 preferably also supports explicit specification or override on the bus compatibility question for the compute engine selected or solicits the assistance of designer 202 in identifying the bus architecture to be employed Column 12, lines 49-53]

### **Applicant's Argue**

Chen fails to explicitly disclose adding additional module/chip description, as claimed.

### **Examiners Response**

The Examiner has considered Applicant's arguments and found them unpersuasive. Rather as rejected Chen supports making an explicit specification to allow the addition and selection of a user module. Furthermore previously cited PSOC designer discloses this feature on page 33.

Regarding claim 13, Chen discloses the method according to Claim 1 further comprising updating the description of the plurality of programmable resources associated with said programmable integrated circuit

[Chen: Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31]

Regarding claim 14, Chen discloses the method according to Claim 13 further comprising adding an additional chip description to the description of the plurality of programmable resource associated with said programmable integrated circuit

[Chen: Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31]

Claim 15 recites the apparatus of method claim 18, thus is rejected for the same reasons as claim 18.

Claims 16, 17 recite similar limitations as claim 2, thus are rejected for the same reasons.

Claim 18 recites similar limitations as claim 1, thus is rejected for similar reasons.

Regarding claim 19, Chen discloses the method according to Claim 18 further comprising:

displaying on a graphical user interface, a first potential placement of said potential placement options; and in response to a user selecting a next placement icon, displaying on said graphical user interface, a second potential placement of said potential placement options [Chen: Figure 7, item 710 showing three memory components].

Regarding claim 20, Chen discloses the method according to Claim 19 wherein potential placement options are displayed using visual attributes and wherein said electronic device is a programmable microcontroller device [Chen: Figure 7, Symble 3G Quartz/ Mcore3 Examples of a compute engine includes but are not limited to microprocessors, digital signal processor, micro-controllers, and the like (Column 11, lines 50-58)].

Regarding claim 21, Chen discloses the method according to Claim 18 wherein said user module requires one pre-existing programmable hardware resource to place [Chen: Figure 7, item 710 memories].

Regarding claim 22, Chen discloses the method according to Claim 18 wherein said user module requires two pre-existing programmable hardware resources to place [Chen: Figure 7, item 710 memories].

Regarding claim 23, Chen discloses the method according to Claim 18 wherein said plurality of pre-existing programmable hardware resources comprise a plurality of pre-existing analog programmable hardware resources and a plurality of pre-existing digital programmable hardware resources [Chen: Figure 2, item 206, IP packages]

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Regarding claim 24, Chen discloses the method according to Claim 18 wherein said comparing automatically prunes out programmable hardware resources that do not satisfy requirements of said user module

[Chen: Thereafter, the selection of designer 202 is received, block 1504. In response, the bus architectures supported by the selected compute engine is retrieved from database 260 and present for selection, block 1506. Upon selection, supported peripherals for the selected bus architecture, with or without the employment of bus bridges 286, are identified and presented for selection by designer 202, block 1508. (Column 14, lines 59-65)].

Claim 25 contains similar limitations as claim 2 thus is rejected for the same reasons.

Claims 26-33 recite the system of method claims 18-25, thus are rejected for the same reasons.

Regarding claim 34 Chen discloses the method as described in claim 1, further comprising:

graphically displaying potential placements location for said first allowed programmable hardware resource

[Chen: For the illustrated embodiment, as shown in FIG. 7, a designer 202 first selects the memory components to be employed from a provided list of available memory items. For the example illustration shown in FIG. 7, several memory components have been added to a memory bus. Specifically, three memory blocks have been selected/added, shown as 710. The example illustration shows the addition of relocatable, banked and standard memories to the SOC design. In addition, the location of each memory block, and their corresponding control blocks, are shown in the memory map 720. Column 14, lines 20-30] Furthermore previously cited PSOC designer discloses this feature on page 33.

Claims 35-37 contain similar limitations as claim 34 thus is rejected for the same reasons.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of PSoC Designer: Integrated Development Environment User Guide Revision 1.09, hereinafter "Guide 1.09".

Regarding claim 8, Chen teaches the method according to Claim 7 further comprising distinguishing disallowed programmable resources. Chen does not expressly teach highlighting the disallowed programmable resource using said graphical user interface.

Guide 1.09 teaches that if you attempt to select a User Module that requires more resources than are currently available, PSoC Designer will not allow the selection.

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to use the user feedback of disallowing the selection with the method of Chen.

The motivation for doing so would have been to give the user visual feedback for the operation being performed.

Regarding claim 9, the combination as applied to claim 9 does not expressly teach that the user feedback is highlighting in gray.

Examiner finds this limitation to be design choice, highlight in gray, or graying out is common and is the default for disallowed user feedback in Windows. Furthermore, the method could just have easily picked any other color for indication of such.

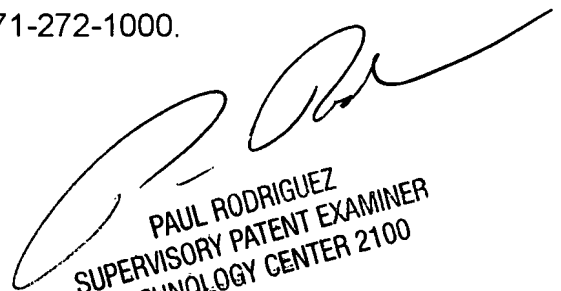
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LRO

  
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